COUNCIL REGULATION (EEC) No 3744/81

of 7 December 1981

concerning Community projects in the field of microelectronic technology

THE COUNCIL OF THE EUROPEAN COMMUNITIES,

Having regard to the Treaty establishing the European Economic Community, and in particular Article 235 thereof,

Having regard to the proposal from the Commission,

Having regard to the opinion of the European Parliament (1),

Having regard to the opinion of the Economic and Social Committee (2),

Whereas microelectronic technology is essential to the development and competitiveness of Community industry as a whole at a time when the European economy must increasingly provide high added value goods and services; whereas, however, the scale and nature of the effort needed to match that of its competitors by 1985 require a Community approach which must include public financial support for collaborative research and development by industry; whereas the Council resolution of 11 September 1979 (3) invites the Commission to examine the possibilities and methods of coordinating national projects in this sector and to submit to the Council specific projects at Community level with a view to promoting microelectronic technology;

Whereas the aid granted should aim at furthering a balanced market and competition situation in Europe and take into consideration the principles expressed in the four-year programme for the development of informatics in the Community, and in particular principles of the ownership of and access to results of supported projects, with particular stress on the importance of an adequate dissemination of goods and other results of supported projects,

(1) OJ No C 144, 15. 6. 1981, p. 69.
(2) OJ No C 353, 31. 12. 1980, p. 4.
(3) OJ No C 231, 13. 9. 1979, p. 1.

HAS ADOPTED THIS REGULATION:

Article 1

In order to attain the Community objectives concerning microelectronic technology, coordination at Community level of the activities undertaken in the Member States in this domain and implementation of joint projects to supplement and reinforce these activities shall be carried out under the conditions set out in this Regulation.

For the purposes of granting national financial support to projects in the fields defined in Article 3, the Member States will in particular encourage projects the execution of which requires major participation on the part of organizations from two or more Community countries, other conditions being equal.

TITLE I

Information and consultation

Article 2

A system for information and consultation concerning initiatives aimed at promoting the diffusion and the development of microelectronic technology and its applications is hereby established between the Member States and the Commission.

Article 3

1. In order to ensure that the consultations provided for in this Regulation are effective, Member States shall, independently of their obligations under the rules of competition, supply the Commission without delay on their own initiative, or at the Commission's request, with all up-to-date relevant advance information of a scientific, economic and financial nature concerning any activities under their authority, both in progress on the date this Regulation enters into force and contemplated after that date, aimed at:

(a) the promotion of applied industrial research and development on equipment, processes, instru-

ments and techniques, both hardware and software, for use in the design, industrial manufacture and testing of advanced integrated circuits;

(b) the dissemination of basic knowledge and the training and education of management and staff specializing in the design, utilization and testing of advanced integrated circuits;

(c) the encouragement of the establishment within the Community of an industry capable of designing and producing the equipment, materials and techniques used in the manufacture of advanced integrated circuits.

They shall also supply the Commission with an appraisal of the result of all these activities.

Confidential company information concerning specific points shall not be covered by this Article.

2. The Commission will ensure that the information concerning the activities referred to in paragraph 1 above is communicated to the Member States.

3. The level of detail of information to be made available to the Commission confidentially, to government agencies of the Member States, or to the public, as well as procedures and measures for making that information available, shall be specified according to the procedure laid down in Article 8.

TITLE II

Joint projects

Article 4

1. The following key research and development projects, coming directly within sectors defined in Article 3 and regarded as having highest priority, shall benefit from Community support under the terms laid down in Article 5.

(I) step and repeat on wafer,

(II) electron beam for direct-writing on wafer,

(III) plasma etching and deposition,

(IV) test equipment,

(V) computer aided design (CAD) for very large scale integration circuitry (VLSI) in the domains of:

1. architecture;
2. language and data structure;
3. testing;
4. device modelling.

2. The technical specifications for the projects specified in paragraph 1 above are set out in the Annex.

3. The Commission shall update the technical specifications as may be required in accordance with the procedure laid down in Article 8.

4. From the beginning of the second year after the entry into force of this Regulation the list reproduced in paragraph 1 may be revised in accordance with the procedure laid down in Article 8 within the limits of the resources available. The Commission may also submit to the Council a proposal for the revision of the Regulation if that is necessary.

TITLE III

Financing procedures

Article 5

1. The European Communities shall provide financial support to the projects specified in Article 4 in the form of subsidies normally covering 30 % of the costs of their execution, but possibly as much as 50 % on the basis of a decision taken in accordance with the procedure laid down in Article 8.

2. The commitment appropriations for the financial support referred to in paragraph 1 above are 40 million ECU. This amount will be included in the budget of the European Communities for 1982.

3. Projects eligible for aid shall meet the following conditions:

— their purpose must be in line with the technical specifications set out in the Annex,

— the projects must be carried out within the Community.

Furthermore:

(a) for projects falling under I to IV of Article 4 (1):

— the applicants must be manufacturers or industrial users established in the Community,

— a sufficient number of sufficiently qualified industrial users not all established in the same Member State and not having financial links with the manufacturer or manufacturers

taking part in the same project must have provided evidence of their interest in participating in the project and in contributing their own resources thereto. This number shall be decided by the Commission, for each project, in accordance with the procedure laid down in Article 8;

(b) for projects falling under V of Article 4 (1):

— the applicants must be universities, research centres or firms established in the Community,

— a sufficient number of sufficiently qualified user firms not all established in the same Member State and not having financial links with each other must have provided evidence of their interest in participating in the project and in contributing their own resources thereto. This number shall be decided by the Commission, for each project, in accordance with the procedure laid down in Article 8.

In applying criteria (a) and (b) above, in cases where resources do not permit two or more otherwise eligible projects of the same nature to be supported, priority shall be given, all other conditions being equal, to the project involving organizations from the largest number of Member States.

4. Once the eligibility of the project has been established under the terms of paragraph 3 (a) or (b) above, all suitably qualified firms established in the Community may take part in the project and apply for the relevant financial support irrespective of their possible financial links with other participants in the same project.

5. Applications shall be addressed to the Commission by those concerned in response to calls for proposals published in the *Official Journal of the European Communities*. These applications shall show evidence that they are justified under the terms of paragraph 3 above and shall provide any other relevant information. The Commission may request any other documents and additional information required for appraisal of the application.

6. The Commission shall act on applications submitted to it within four months.

7. Without prejudice to the powers of the Court of Auditors pursuant to Article 206a (3) of the Treaty, the Commission may carry out investigations on the spot or inquiries into the operations financed, according to the conditions specified in the contracts regulating the financing of the projects.

TITLE IV

General provisions

Article 6

1. A Consultative Committee, hereinafter called 'the Committee', is hereby set up for projects promoting microelectronic technology. It shall consist of representatives of the Member States, who may be assisted by experts or advisers depending on the nature of the projects under consideration, with a Commission representative as chairman.

2. The proceedings of the Committee shall be confidential.

3. The Committee shall adopt its own rules of procedure.

4. Secretarial services for the Committee shall be provided by the Commission.

Article 7

The Commission may consult the Committee on any matter falling within the scope of this Regulation and must in particular consult it on:

— the level of detail of the information concerning national activities to be supplied confidentially to the Commission in accordance with Article 3,

— the level of detail of the information to be published or notified to the government agencies of Member States,

— the procedures for making the information collected available to the Member States,

— the updating of the technical specifications for projects potentially eligible for financial support,

— the minimum number of firms required to make a project eligible for financial support,

— the appraisal of applications and the granting of financial support.

Article 8

1. Where the procedure laid down in this Article is to be followed, the matter shall be referred to the Committee by its chairman, either on his own initiative or at the request of the representative of a Member State.

2. The Commission representative shall submit a draft of the measures to be taken. The Committee shall give its opinion on the draft Decision within two months. Its decisions shall be taken by a majority of 45 votes. Within the Committee the votes of the Member States shall be weighted in accordance with Article 148 (2) of the Treaty. The chairman shall not vote.

3. The Commission shall adopt the draft where it is in accordance with the opinion of the Committee. Where the draft Decision is not in accordance with that opinion or where no such opinion is issued, the Commission shall without delay make a proposal to the Council in the form of a draft Decision. The Council shall act by a qualified majority.

Article 9

Each year the Commission shall forward to the European Parliament and to the Council a report on the development of the activities in the Community falling within the scope of this Regulation.

Article 10

This Regulation shall enter into force on 1 January 1982.

It shall apply until 31 December 1985.

This Regulation shall be binding in its entirety and directly applicable in all Member States.

Done at Brussels, 7 December 1981

For the Council

The President

CARRINGTON

ANNEX

OUTLINE TECHNICAL SPECIFICATION OF PROJECTS AND ACTIVITIES FOR WHICH FINANCIAL SUPPORT IS BEING PROPOSED UNDER THE TERMS OF THE REGULATION

I. STEP AND REPEAT ON WAFER

Direct optical stepping technology

Direct optical stepping machines should be available in production with the characteristics listed below by the end of 1982:

— wafer size: up to six inches,

— die size: 1 cm^2,

— minimum line widths: 1·25 μm on the wafer (1·1 μm on the resist),

— automatic registration: 0·1 μm,

— throughput 50 × four-inch wafers per hour at 1 cm^2 field with insertion of five test patterns and auto-registration at each chip; addition of a reticle magazine.

Individual times should be given in the description of the equipment including the time to insert test patterns. Registration should be programmable (per individual exposure — per block — per wafer). Minimum allowable size of alignment marks should be given.

It is considered desirable that machines could be supplied in 1983 with an improved throughput of 50 × six-inch wafers per hour and improved resolution of 1·0 μm minimum line width on wafer.

II. ELECTRON BEAM FOR DIRECT-WRITING ON WAFER

Electron beam direct-writing equipment

E-beam machines capable of:

— wafer size: six inches,

— throughput: 15 to 20 layers per hour at 1 μm,

— die size: no limitation,

— minimum feature size: 0·5 μm,

— spot size: variable,

— registration accuracy: 0·1 μm.

This equipment should also be suitable for reticle and mask making. Prototype machines meeting all these requirements apart from speed must be available within 1983.

III. PLASMA ETCHING

A. **Minimum performances of the equipment**

— *Materials to be etched*

— SiO_2, doped and undoped.

— Si_3N_4.

— Polysilicon, doped and undoped.

— Silicides and polycides.

— Aluminium and aluminium alloys.

— Other metals for contacts and interconnections.

— Organic polymers for multilevel resists and multilevel metallization.

— *Structures to be etched in production*

— Pitch (line plus spacing): 3 µm.

— Minimum linewidth: 1 to 1·5 µm.

— Precision: + or — 10 % of linewidth for the critical structures.

— *Selectivity and anisotropy*

The selectivity has to be adequate and for each layer it should be possible to etch completely anisotropically.

— *Throughput*

The minimum throughput should be 50 wafers per hour for the slowest process. The slowest process will probably be the etching through 0·8 µm of thermal SiO_2 with a selectivity of 10 : 1 over Si and with a pitch of 3 µm. The etching of other layers (e.g. 0·4 µm undoped polysilicon over SiO_2) should be much faster.

B. **Design of the equipment**

We consider a parallel plate reactor with the following features:

— *Design concept*

Most important is the use of a modular design concept so that the equipment can be optimally adapted for each application.

— *Load lock*

Undesired species (e.g. water vapour) should be blocked from the reaction chamber and post-etching effects must be avoided. This can be reached with a vacuum lock containing the cassettes. Stripping of the photoresist in the unload-lock should be considered as an option.

— *Electrode and chamber construction*

— Individually driven thermostats for upper and lower electrode and for the reaction chamber. The range for temperature control is 15 to 100 °C standard and up to 150 °C as an option.

— Electrode distance adjustable between: 5 to 70 mm (batch oriented system),
5 to 70 mm (single wafer system).

— The electrode assembly must be suited for operation at high frequencies (until 27·12 MHz), e.g. avoid parasitic plasma anywhere in the reactor.

— Both parallel plasma etching (PE) and reactive ion etching (RIE) must be possible in the system (anode and cathode coupling).

— *Vacuum design*

— The region of interest is between 10 mTorr and 10 Torr.

— Adjustable pumping speed.

— Automatic and manual pressure control with simple switching between the two modes.

— Use of non-corrosive materials for seals (fittings, O-rings) and tubing.

— *Gas cabinet*

Flexible handling of one to three gasses with one to three mass flow controllers, preferentially extendable to five gases (number of gases is an option).

— *Controls*

— The following parameters must be controllable:
gasline(s) in use,
flowrate,
process time,
time to stabilize,
time to overetch,
RF power,
temperature of both electrodes,
voltage on electrode.

— The electrical signal from the sensors (pressure sensor, etc.) must be easily accessible (e.g. on a standard plug) for process monitoring.

— At least one window to look into the plasma and additional flange(s) to hook up some analytical tools for process monitoring should be available.

— *Automatic etching control system*

— A keyboard and necessary memory for the step by step command of the process or the maintenance sequence.

— A plug-in PROM, user programmed, for automatic etching.

— *Wafer handling*

Automatic wafer handling, cassette to cassette load and unload without wafer damage or contamination.

The system should handle three inch wafers of up to 150 mm diameter.

— *Maintenance and safety*

— Easy dismantling for cleaning and repair.

— Standardization of flanges, seals, plugs, etc., and spare parts.

IV. TESTING EQUIPMENT

European testers for integrated circuits should be developed with the following characteristics:

— of the integral analog/digital type,

— of modular design, in order to be adaptable to both development and production testing tasks,

— development in two phases, as far as the digital part is concerned. The first step should be a tester for clock-rates of 10 to 20 MHz, the second step aiming at 50 to 100 MHz. This stepwise development has the advantage that the technological know-how built up in the first phase can be used to tackle the problems that have to be faced in the second

development round. Moreover, the high speed test development can thus be adapted to the developing requirements of the European IC industry in the high speed bipolar circuits,

— testing of devices with an increasing number of pins (from 64 to 128),

— substantial parts of the test system have to be 'ECL-specific',

— testing of memory devices alone has been excluded, however 'on-the-chip' memories are becoming increasingly important and therefore their testing has to be covered,

— one single high level test language concept should be supplied for the different tester configurations.

V. CAD FOR VLSI

1. Architecture

The problems to be tackled are the disciplines of specification, simulation and testing at the architectural design phase and the architectural strategies like error management and structured logic. The following activities appear to be required:

— Improvement in knowledge of computer techniques by VLSI designers through:

(a) transfer of know-how from computer manufacturers;

(b) better integration of computer science and electronic engineering training in universities.

— Research on:

(a) linking of behavioural and structural design by development of suitable languages and simulators;

(b) synthesis of logic from RTL description;

(c) error management including fault-tolerant aspects of VLSI architecture;

(d) structured logic including minimization for PLAs (programable logic arrays) and automatic programming of PLAs and ROMs (read only memories);

(e) firmware generation and simulation aids;

(f) parallel processing machines for signal processing.

2. Language and data structure

2.1. *Design data management*

Conventional graphic IC design systems are based upon a bottom up representation of the circuit being designed. This is considered inadequate for coping with the problems of VLSI design, and instead, a specification of a file management or design management system must be formulated with respect to the following purposes:

(a) to aid the management of a large number of files representing alternative representations of many modules of a system;

(b) to protect the integrity of a design involving a team effort;

(c) to manage design modifications;

(d) to aid re-partitioning of a design;

(e) to manage the provision of design documentation.

Research projects must be initiated which will enhance the normal filing system or operating system to provide the above facilities. The smallest unit of data in a transaction will be a complete file, and so conventional data bases are not appropriate. The implementation must be carried out with portability in mind. A standard language must be used with well-defined interfaces to standard filing systems. This project should be a joint project between IC designers, CAD tool specialists, and computer scientists.

2.2. *User interface*

Some design activities are highly interactive and demand a guaranteed fast response from the computer while not demanding a very powerful computer. An example is design specification using graphical techniques. Such activities can be supported on a small computer dedicated to a single user. Other activities are not primarily interactive, but do require very powerful computing facilities. An example is simulation. Such activities need powerful time-shared systems.

It is important that the computers supporting these related activities should be intimately connected. Techniques for controlling tasks split between two or more computers, and for allowing flexible movement of data between these tasks, should be investigated. General principles applicable to a wide range of hardware should be established.

The present trend in hardware design specification is to use text based language descriptions which are convenient for expressing the hierarchical structure, modularity, and repetitivity which is inevitable with VLSI. However, designers still tend to think in terms of diagrams, and graphical aids will continue to be valuable in the design process. A project ought to be launched to investigate methods of combining textual and graphical representations allowing each to be converted automatically into the other, so that the most appropriate interface can be freely chosen at each part of the design process.

2.3. *Simulation*

Software tools for simulation, test and verification have to span the design spectrum from RTLs down to transistor level. Activity should be directed towards the development of a flexible multilevel structural description language for NMOS and CMOS VLSI. Automatic compiler generation into the syntax of presently used single level tools and, more importantly, directly into the data structure of mixed mode simulators needs investigation. Mixed mode simulation techniques need considerable attention in the area of data structures, algorithms, and models.

It is strongly recommended to pay special attention to VLSI network analysis rather than pure simulation in order to reduce design time and ensure design correctness. This is a completely new research domain which looks entirely feasible based on the data structures and algorithms of presently existing mixed mode simulators.

2.4. *Verification*

Instead of intensive verification of manually performed or interactive design steps, the goal should be to automate as much as possible (silicon compilation, standard cell technique, etc.) to make verification unnecessary. To find a solid basis for the use or creation of such tools, a study should be initiated which compares the different approaches as well as different handcrafted layouts to find objective criteria for the fundamental principles of efficiency in layout.

The hierarchical design of VLSI is obvious. The verification between the different levels of hierarchy is a problem but cannot be avoided. In spite of the hierarchy, the complexity and amount of data is enormous and with today's tools leads to uneconomic computer times. Therefore, further candidates for research and development are dedicated hardware modules (e.g. design rule checkers, pattern memory plus counters and shift registers, or hardware language processors which produce the appropriate data structures).

2.5. *Influence of new computer architectures*

On the basis of the assumption that:

— software is now expensive and should be optimized while hardware is cheaper and can be used more freely,

— in the past few years a lot of high performance parallel processors have been developed and implemented,

— the architecture of a machine should fit the problem it is to solve,

investigation in the following two areas is proposed:

(a) development of new parallel algorithms and new data structures in any CAD branch, to exploit and implement the maximum parallelism;

(b) study of new special pufpose hardware processor to be interfaced with currently existing computer systems to improve part of their performance by at least one order of magnitude.

3. **Testing: summary of recommendations**

The team on testing recommend organizing future work in accordance with three main areas and the related topics listed below.

Main area of activities

	Research	Specification and evaluation	Development
1. TEST DATA GENERATION			
— Functional level testing (methods and strategies)	*		
— Element level ATPG	*		
— ATPG for LSI cells, regular logic, etc.	*		
— Fault types and models	*		
— Fault simulation strategies	*		
— Modular ATPG system		*	*
— Language for MTPG		*	*
— Integrated ATDG system		*	*
2. DESIGN FOR TESTABILITY			
— Partitioning	*		
— RAM design for testability	*		
— Microprogrammed units	*		
— Design for testability general techniques	*		
— Hardware implemented self-testing	*		
— Software/firmware self-testing	*		
3. DATA ACQUISITION AND DATA MANAGEMANT			
— DADM system		*	*
— Program development tools		*	*

4. Device modelling: summary of recommendations

The present report on device modelling covers three main areas:

— numerical device simulation,
— analytical models,
— table models.

For each of them, the main recommendations are summarized below.

4.1. *Numerical device simulation*

The main target of this subproject is that of stimulating European research centres and laboratories to develop advanced device-simulation packages, and make them available to European IC manufacturers. This should allow reaching an independence with respect to American and Japanese counterparts. The need for such an activity stems from the fact that, due to the importance of two-, and even three-dimensional effects, numerical device simulation represents the only predictive tool which can practically be used for device design. It is therefore recommended that at least four simulation packages be developed, namely:

— 2-D MOSFET simulator,
— 2-D simulator for bipolar devices,
— 3-D MOSFET simulator,
— 3-D simulator for bipolar devices.

For each of them, detailed specifications have been defined concerning the physical phenomena to be incorporated in the program, the physical and geometrical device structure, and I/O graphical capabilities.

4.2. *Analytical models (MOSFETs only)*

An activity in this area is essential for two main reasons: from the one hand analytical models trading off accuracy and simplicity are mostly suited for circuit designers in CAD circuit simulation programs; on the other hand, the functional dependence of relevant electrical parameters on geometrical and physical device structure is most easily identified in analytical models, which can, therefore, provide some insight in the physical phenomena occuring within a device.

The following analytical models should be developed:

Surface channel MOSFETs	long channel, low voltage (level 1) long channel, high voltage (level 2) short channel, low voltage (level 3) short channel, high voltage (level 4)
Buried channel MOSFETs	long channel (level 1) short channel (level 2)

4.3. *Physical model*

Again, detailed specifications are provided for each of the above models. In addition to the development of the models, the problem of parameter identification should be tackled and solved, especially as far as charges (or capacitances) are concerned.

4.4. *Table models*

The need for table models has been recognized for timing simulation purposes. In such simulators, the capacitances are rather poorly handled, being assumed as constants; therefore, the activity in this area should aim at developing tables for both currents and capacitances. The most important problem to be solved is that of providing the scaling rules, while maintaining the computational simplicity which is needed in order to strongly reduce the CPU time, with respect to that needed with analytical models.